



Example of Flexible Multi-Layer Substrates with High Density Copper Wiring (top) and Embedded ICs (bottom)

## Flexible High Density Multi-Layer Substrates with embedded ICs

Fraunhofer IZM offers a variety of processes for the manufacturing of high density multi-layer flex substrates. The fabrication approach features the capabilities of Fraunhofer IZMs well established wafer level redistribution technology which is applied on rigid temporary carrier wafers.

The high density wiring layers are generated in semi-additive technology using seed layer deposition by PVD, mask aligner technology for pattern definition in photo resist as well as electro-chemical deposition of metals. Typical copper is used as wiring metallization with up to 5  $\mu\text{m}$  track height and line pitches below 20  $\mu\text{m}$ .

The inter dielectric layers with micro vias are fabricated by spin coating, lithographic structuring and cure of photo sensitive polyimide precursors. A multi-layer build up is obtained by sequential alternated processing of polyimide and metall layers. With the current technology flexible substrates with up to four internal metal routing layers were fabricated so far which have a thickness of approx. 50  $\mu\text{m}$ . The technology also allows the embedding of thin IC components inside such flex layers. To enable that, approx. 20  $\mu\text{m}$  thin ICs are die bonded onto one of the initial polymer layers during the flex build-up. A following overcoating with polymer completely covers the thin ICs. The chip

IOs are accessed by lithographic structuring of vias into the photo sensitive polymer layer. The next redistribution layer interconnects the chip IOs electrically to the wiring of the flex.

As further feature, electrical through conatcts through the flex substrates can be realized. With that option interconnections from the bottom to the top side of the flex substrates become possible.

In order to accommodate the flex substrate to any desired assembly and interconnection process such as soldering, wire bonding or thermo compression bonding using conductive adhesives custom specific pad metallizations like Cu, CuSn, Au, NiAu, AuSn or AgSn can be fabricated.

Based on standard redistribution technology additional features like integrated passive components such as inductors, capacitors and resistors can be implemented into the multi-layer wiring structure of the flex substrates.

After the complete processing of the multi-layer build up it will be detached from the temporary carrier wafer using a special desined high speed de-bonding process. By using the described technology fully custom specific foldable or stackable flexible multi layer substrates with arbitrary shapes and forms as well as chemical and high temperature stability can be manufactured.

### Fraunhofer Institut für Zuverlässigkeit und Mikrointegration IZM

Gustav-Meyer-Allee 25  
13355 Berlin  
Deutschland

#### Kontakt

Kai Zoschke  
Telefon +49 30 46403-221  
kai.zoschke@izm.fraunhofer.de

Dr. Michael Schiffer  
Telefon +49 30 46403-234  
michael.schiffer@izm.fraunhofer.de

[www.izm.fraunhofer.de](http://www.izm.fraunhofer.de)